Notice of Allowability	Application No.	Applicant(s)	
	10/614,067	LEEDY, GLEN J.	
	Examiner	Art Unit	
	Pamela E. Perkins	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *the amendment filed on 14 September 2006*.

2. ☒ The allowed claim(s) is/are *88-142,146-154,156-164 and 166-171*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. **THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date 9/14/06
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

This office action is in response to the filing of the amendment on 14 September 2006. Claims 88-142, 146-154, 156-164 and 166-171 are pending; claims 143-145, 155 and 165 have been cancelled.

Allowable Subject Matter

Claims 88-142, 146-154, 156-164 and 166-171 allowed.

Reasons for Allowance

The following is an examiner's statement of reasons for allowance: referring to claims 88, 97 and 101, prior art does not anticipate, teach, or suggest a plurality of monolithic substrates having integrated circuits formed thereon and stacked in layers such that each layer comprises only one of the substrates, wherein at least one of the plurality of substrates is a substantially flexible substrate, and wherein a major portion of the monolithic substrate is removed.

Referring to claim 125, prior art does not anticipate, teach, or suggest wherein at least one substrate of the first and second substrates has memory circuitry formed thereon, the memory circuitry having a plurality of memory locations including at least one memory location used for sparing, wherein data from the at least one memory location on the at least one substrate that has memory circuitry formed thereon is used instead of data from a defective memory location on the least one substrate that has memory circuitry formed thereon.

Referring to claims 128, 146 and 156, prior art does not anticipate, teach, or suggest wherein at least one substrate of the first and second substrates has reconfiguration circuitry.

Referring to claim 130, prior art does not anticipate, teach, or suggest the memory array having a plurality of memory storage cells, a plurality of data lines, and a plurality of gate lines, each memory storage cell stores data value and has circuitry for coupling that data value to one of the plurality of data lines in response to receiving a gate control signal from one of the plurality of gate lines; circuitry that generates the gate control signal in response to receiving an address, including means for mapping addresses to gate lines; and controller that determines one of the plurality of memory cells is defective and alters the mapping to eliminate references to the one of the plurality of memory cells that is defective.

Referring to claim 131, prior art does not anticipate, teach, or suggest at least one controller substrate having logic circuitry formed thereon; at least one memory substrate having memory circuitry formed thereon; a plurality of data lines and a plurality of gate lines on each memory substrate; an array of memory cells on each memory substrate, each memory cell stores a data value and has circuitry that couples the data value to one of the plurality of data lines in response to selecting of one of the plurality of gate lines; a gate line selection circuit that enables a gate line for a memory operation, wherein the gate line selection circuit has programmable gates to receive address assignments for at least one of the plurality of gate lines and wherein the address assignments for determining which the plurality of gate lines is selected for

each programmed address assignment; and controller substrate logic that determines one memory cell of the array of memory cells is defective and alters the address assignments of the plurality of gate lines to remove references to the gate line that causes the defective memory cell to couple a data value to one of the plurality of data lines.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Pamela E. Perkins whose telephone number is (571) 272-1840. The examiner can normally be reached on Monday thru Friday, 8:30am to 5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Zandra Smith can be reached on (571) 272-2429. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PEP
25 September 2006

Zandra V. Smith
Supervisory Patent Examiner
28 Sept. 2006